UNITED STATES PATENT AND TRADEMARK OFFICE

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10/625,365	07/23/2003	Richard W. Adkisson	200300031-2	8221

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EXAMINER
DSOUZA, JOSEPH FRANCIS A

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>02 April 2008</u>.
2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1 -7, 9 - 24</u> is/are pending in the application.
     4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☒ Claim(s) <u>1 - 7, 9 - 11</u> is/are allowed.
6)☒ Claim(s) <u>12 - 24</u> is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
     a)☐ All   b)☐ Some *   c)☐ None of:
       1.☐ Certified copies of the priority documents have been received.
       2.☐ Certified copies of the priority documents have been received in Application No. _____.
       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
     Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1.   Applicant's arguments with respect to independent claims 12, 19 and 23, filed

4/2/2008 have been fully considered but they are not persuasive.

- Argument: Applicant argued that Garcia does not teach receiving data blocks having

   intervals and sending contiguous data blocks (Remarks 4/2/2008, page 23, 1st full

   paragraph, 1st 5 lines).

   Response: Examiner respectfully disagrees. Garcia discloses that there are intervals

   between the bits (column 4, lines 36 – 49; wherein from the description it is obvious

   that there are gaps intervals between the bits.

- Argument: Applicant argued that Garcia does not disclose data blocks for

   transmission from a first portion of data block are temporarily stored and a second

   portion of the data blocks are provided without queuing (Remarks 4/2/2008, page

   23, 1st full paragraph, middle of page).

   Response: Examiner respectfully disagrees. Examiner is using Audityan to disclose

   the queuing limitation (see rejection of claim 3 in last Office Action)

- Argument: Applicant argued that Garcia does not disclose advance notice of the

   paragraph).

   Response: Examiner respectfully disagrees. Firstly, as shown in Fig. 4, the HIGH

   STROBE indicates the position of the dead cycle. The position is indicated at the

time of the dead cycle. Advance notification is a trivial thing to one of ordinary skill in the art, since once can easily incorporate a simple delay element in the appropriate path to make the HIGH STROBE appear before the actual dead cycle. Secondly, Applicant has stated advance notice as being "0 – (N – 1) cycles" prior to the dead cycle (see claim 11). "0" advance is disclosed by Garcia.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.   Claims 12 - 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Garcia et al. (US 6,084,934)** in view of **Audityan et al. (US 6,317,806).**

Regarding claim 12, Garcia discloses a circuit for effectuating the transfer of data blocks having intervals to a synchronizer disposed between two clock domains, comprising (Abstract, 1st 4 lines; column 1, lines 6 – 9; Fig. 1, element 14 clock rate CLK Y and element 12 at clock rate CLK X),

whereby said data blocks are transmitted to said synchronizer as a packet of contiguous data blocks relative to said at least one dead cycle (Fig. 4, data blocks transmitted according to HIGH STROBE).

Garcia doesn't disclose means for receiving and temporarily storing a first set of data

blocks having intervals and a second set of blocks and selecting between them.

In the same field of endeavor, however, Audityan discloses means for receiving and

temporarily storing a first set of data blocks having intervals (Fig. 1, element 51 output

that controls the mux 19 which receives data from the queue 16; column 5, lines 25 –

39, 52 – 60; column 7, lines 17 – 27; wherein the control logic is interpreted as the

decoder 19, the data control signals are interpreted as the output of the decoder that

control the selection from the queue 16) and means for selecting between said first

portion of said data blocks and a second portion of said data blocks having intervals

provided without queuing (Fig. 1, elements 19, 51; column 5, lines 25 – 39, 52 – 60;

column 7, lines 17 – 27; wherein the mux is element 19 that selects one of the queue

entries).

 Therefore it would have been obvious to one having ordinary skill in the art, at the time

the invention was made, to use the method, as taught by Audityan, in the system of

Garcia because this would allow the appropriate data element from the queue to be

selected, as disclosed by Audityan (same column, line numbers as above).

Claim 13 is analyzed similar to limitations in claim 12, since claim 12 discloses atleast

one queue.

Claim 14 is analyzed similar to limitations in claim 12, since the rejection for claim 12

discloses a queue that uses a FIFO system.

Claim 15 is analyzed similar to limitations in claim 12, since the rejection for claim 12

discloses a mux to do the selection

Claim 16 is analyzed similar to limitations in claim 12, since the rejection for claim 12

discloses the HIGH STROBE that is used to indicate the position of the dead cycle.

Claims 17 and 18 are analyzed similar to limitations in claim 12, since the rejection for

claim 12 discloses transfer between two clock domains.

Regarding claim 19, Garcia discloses a system for effectuating the transfer of data

blocks having intervals across a clock boundary between a first clock domain and a

second clock domain (Abstract, 1st 4 lines; column 1, lines 6 – 9; Fig. 1, element 14

clock rate CLK Y and element 12 at clock rate CLK X), wherein said first clock domain

is operable with a first clock signal and said second clock domain is operable with a

second clock signal (Figs. 1 & 2, CLK y and CLK X) , said first and second clock signals

having a ratio of N first clock cycles to M second clock cycles, wherein N/M>1 (Fig. 4,

CLK Y comprising 9 clock cycles to CLK X comprising 8 clock cycles; wherein N = 9 and

M = 8) , comprising:

generating notice indicative of the location of at least one dead cycle occurring between

a first clock signal and a second clock signal used for transmitting data across a clock

boundary (Fig. 2, element 16; Fig. 3; Fig. 4, element HIGH STROBE; wherein the HIGH

STROBE output indicates the position of the dead cycle, as shown in Fig. 4);

receiving packet data and said notice indicative of the location of said at least one dead

cycle, said packet data including said data blocks having intervals (Fig. 2, element 16;

Fig. 3; Fig. 4, element HIGH STROBE; wherein the HIGH STROBE outputs and the

HIGH STROBE output indicates the position of the dead cycle, as shown in Fig. 4);

calculating the optimal time to send said packet data relative to the location of said at

least one dead cycle (column 4, line 61 – column 5, line 7);

and transmitting ordered contiguous data blocks about said at least one dead cycle to a

CLKI-to-CLK2 synchronizer for transmission to receive circuitry disposed in said second

clock domain (column 4, line 61 – column 5, line 7).

As stated in "Response to Arguments" above Garcia shows in Fig. 4, the HIGH STROBE

indicates the position of the dead cycle. The position is indicated at the time of the dead

cycle. Therefore it would be obvious to one of ordinary skill in the art to incorporate a

simple delay element in the appropriate path to make the HIGH STROBE appear before

the actual dead cycle.

Regarding claim 20, Garcia discloses at least one dead cycle comprises N-M dead

cycles (Fig. 4, CLK Y and CLK X waveforms; where CLK Y has 9 clock cycles and CLK

X has 8 clock cycles, giving 1 dead cycle).

Regarding claim 21, Garcia discloses the dead cycle control signal is provided 0 to N-1

cycles prior to said dead cycle (see Response to Arguments above, 3rd bullet).

Regarding claim 22, Garcia discloses the operation of transmitting ordered contiguous data blocks about said dead cycle further comprises transmitting at least one of said data blocks adjacent to said dead cycle (Fig. 4, HIGH STROBE signal shows data positioned near DEAD CYCLE).

Claim 23 is directed to apparatus of the same subject matter claimed in method/steps claim 19 and therefore, is rejected as explained in the rejection of claim 19 above.

Claim 24 is directed to apparatus of the same subject matter claimed in method/steps claim 12 and therefore, is rejected as explained in the rejection of claim 12 above.

Conclusion

4.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

5.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Adolf DSouza whose telephone number is 571-272-

1043. The examiner can normally be reached on Monday through Friday from 8:00 AM

to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, David Payne can be reached on 571-272-3024. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Adolf DSouza
Examiner
Art Unit 2611

AD

/David C. Payne/

Supervisory Patent Examiner, Art Unit 2611